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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,013	11/20/2003	Giovanni Campardo	I02057-US (2110-84-3)	2787
996	7590	05/02/2005	EXAMINER	
GRAYBEAL, JACKSON, HALEY LLP			HUR, JUNG H	
155 - 108TH AVENUE NE			ART UNIT	
SUITE 350			PAPER NUMBER	
BELLEVUE, WA 98004-5901			2824	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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**Office Action Summary**

Application No.

10/720,013

Applicant(s)

CAMPARDO ET AL.

Examiner

Jung (John) Hur

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 14-27 is/are allowed.
- 6) ☒ Claim(s) 1-7 and 13 is/are rejected.
- 7) ☒ Claim(s) 8-12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: search history.

## **DETAILED ACTION**

### ***Preliminary Amendment***

1. Acknowledgment is made of applicant's Preliminary Amendment, filed 15 March 2004.

The changes and remarks disclosed therein were considered.

No claims have been cancelled or added. Therefore, claims 1-27 are pending in the application.

### ***Specification***

2. Claims 1, 4 and 14 are objected to because of the following informalities:

In claim 1, it is not clear whether "a respective signal line" in line 10 is same as one of "a plurality of memory cell access signal lines" in line 3. In view of the specification and the drawings, it will be understood as referring to one of "a plurality of memory cell access signal lines" in line 3.

Claim 4 recites "said lines...are bit lines" implying that the signal lines are bit lines; however, claim 5 in lines 1-2 recites "said signal lines are global bit lines and said bit lines are local bit lines" (emphasis added). Therefore, claim 4 is not clear. Claim 4 will be understood as reciting a further limitation of "bit lines" in the memory.

In claim 14, line 3, the parenthesis "(" should be removed.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

Art Unit: 2824

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

In addition, the following are quotations from MPEP that further form the basis for the rejections under this section:

"[T]he discovery of a previously unappreciated property of a prior art composition, or of a scientific explanation for the prior art's functioning, does not render the old composition patentably new to the discoverer." *Atlas Powder Co. v. Ireco Inc.*, 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1947 (Fed. Cir. 1999). Thus the claiming of a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable. *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977). See MPEP §2112 I.

There is no requirement that a person of ordinary skill in the art would have recognized the inherent disclosure at the time of invention, but only that the subject matter is in fact inherent in the prior art reference. *Schering Corp. v. Geneva Pharm. Inc.*, 339 F.3d 1373, 1377, 67 USPQ2d 1664, 1668 (Fed. Cir. 2003). See MPEP §2112 II.

While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). See MPEP §2114.

A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See MPEP §2114.

4. Claims 1-7 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Tedrow et al. (U.S. Pat. Appl. Pub. No. 2002/0085423).

Tedrow, for example in Figs. 2 and 3, discloses a semiconductor memory comprising: a plurality of memory cells (EEPROM cells in Fig. 2), arranged in a plurality of lines (for example, vertically); a plurality of memory cell access signal lines (vertical global bit lines connected to the Global Y Selects), each one associated with at least one respective line of

Art Unit: 2824

memory cells (via Local Y Selects), for accessing the memory cells of the at least one respective line of memory cells (one vertical set of cells), each signal line having a capacitance intrinsically associated therewith (inherent),

characterised by further comprising: a plurality of volatile memory cells (each including the capacitance associated with a global bit line), each volatile memory cell having a capacitive storage element (associated with the global bit line capacitance), each volatile memory cell being associated with a respective signal line (a respective global bit line), the capacitive storage element of each volatile memory cell comprising the capacitance intrinsically associated with the respective signal line (inherent); in which said capacitance is a parasitic capacitance intrinsically associated with the signal line (inherent);

further comprising: a signal line selector (Global Y Selects) adapted to selecting the signal lines for accessing the memory cells, and a volatile memory cell selector for selecting the volatile memory cells, the volatile memory cell selector comprising the signal line selector (i.e., Global Y Selects as the access transistors for the volatile memory cells);

further comprising bit lines (local bit lines in Fig. 2); in which said signal lines are global bit lines and said bit lines are local bit lines of the memory (see Fig. 2), each global bit line being associated with at least two local bit lines (from each block in Fig. 3), and comprising a local bit line selector (Local Y Selects in Fig. 2) for selectively connecting the local bit lines to the respective global bit line; in which said memory cells are arranged to form at least two memory sectors (blocks in Fig. 3), the plurality of local bit lines associated with any global bit line comprising at least one local bit line in each of the at least two memory sectors (see Figs. 2 and 3); in which the local bit line selector keeps the local bit lines disconnected from the respective

Art Unit: 2824

global bit line when accessing the volatile memory cells (the Local Y Selects are capable of disconnecting the local bit lines from the respective global bit lines; see Fig. 2); and in which said memory cells are non-volatile memory cells (EEPROM cells in Fig. 2).

*Allowable Subject Matter*

5. Claim 14-27 are allowed.

Claim 8-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 8, the prior arts of record do not disclose or suggest a memory as recited in claim 8, and particularly, a circuit for writing data into the volatile memory cells (with the access signal line capacitance used as a storage capacitor).

Regarding claim 14, the prior arts of record do not disclose or suggest a method as recited in claim 14, and particularly using the capacitive storage element associated with an access signal line for volatily storing second data (as distinguished from the first data).

Regarding claims 15 and 25, the prior arts of record do not disclose or suggest a memory as recited in claim 15 or 25, and particularly, read-write circuitry operable in a second read mode and a second write mode to select a bit line and isolate all memory cells from the selected bit line, and to sense the bit line to detect data stored on the selected bit line or to transfer data into the selected bit line.

Art Unit: 2824

Regarding claim 21, the prior arts of record do not disclose or suggest a method as recited in claim 21, and particularly storing data on the bit lines of the array (i.e., storing data such that the data would be available for reading later).

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Deguchi et al. (U.S. Pat. No. 4,760,556) discloses an EEPROM with a capacitor.

Cho (U.S. Pat. No. 5,025,421) discloses a dual RAM with DRAM and SRAM.

Forbes et al. (U.S. Pat. No. 6,141,248) discloses an EEPROM with a capacitor.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870.

The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2824

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh



**ANH PHUNG  
PRIMARY EXAMINER**